

100G DSFP Active Optical Cable

Product Features

- Compliant with IEEE 802.3cd
- 2x53.125GBd PAM4 transmitter and PAM4 receiver
- Maximum link length of 70m on OM3 MMF and 100m on OM4 MMF with FEC
- 2 channels 850nm VCSEL array
- 2 channels PIN photo detector array
- Single +3.3V power supply
- Power consumption <3.5W
- Operation case temperature: 0~70°C
- RoHS10 compliance, and Class 1 laser safety



Application

- 100G Ethernet

Absolute Maximum Ratings

Parameter	Units	Min.	Typical	Max.	Note
Storage Temperature	°C	-45		85	
Operating Relative Humidity	%	5		85	
Power Supply not Damaged Voltage	V	-0.3		3.6	

Recommended Operating Conditions

Parameter	Units	Min.	Typical	Max.	Note
Operating Case Temperature	°C	0		70	1
Power Supply Working Voltage	V	3.135	3.3	3.465	
Power Consumption	W			3.5	
Bit Rate	Gbps		106.25		

Note:

1. Case Temperature here is depending on module case around LD, NOT the environmental temperature.

Electrical Specifications

Parameter	Units	Min.	Typical	Max.	Note
Transmitter					
Data Input Swing Differential/TX	mV	50	-	1500	
Date Differential Impedance	Ω	90	100	110	
Receiver					
Data Output Swing Differential/RX	mV	-	-	900	
Date Differential Impedance	Ω	90	100	110	
Bit Error Ratio				2.4E-4	1

Note: 1. PRPS31Q@26.5625GBd. Pre-FEC

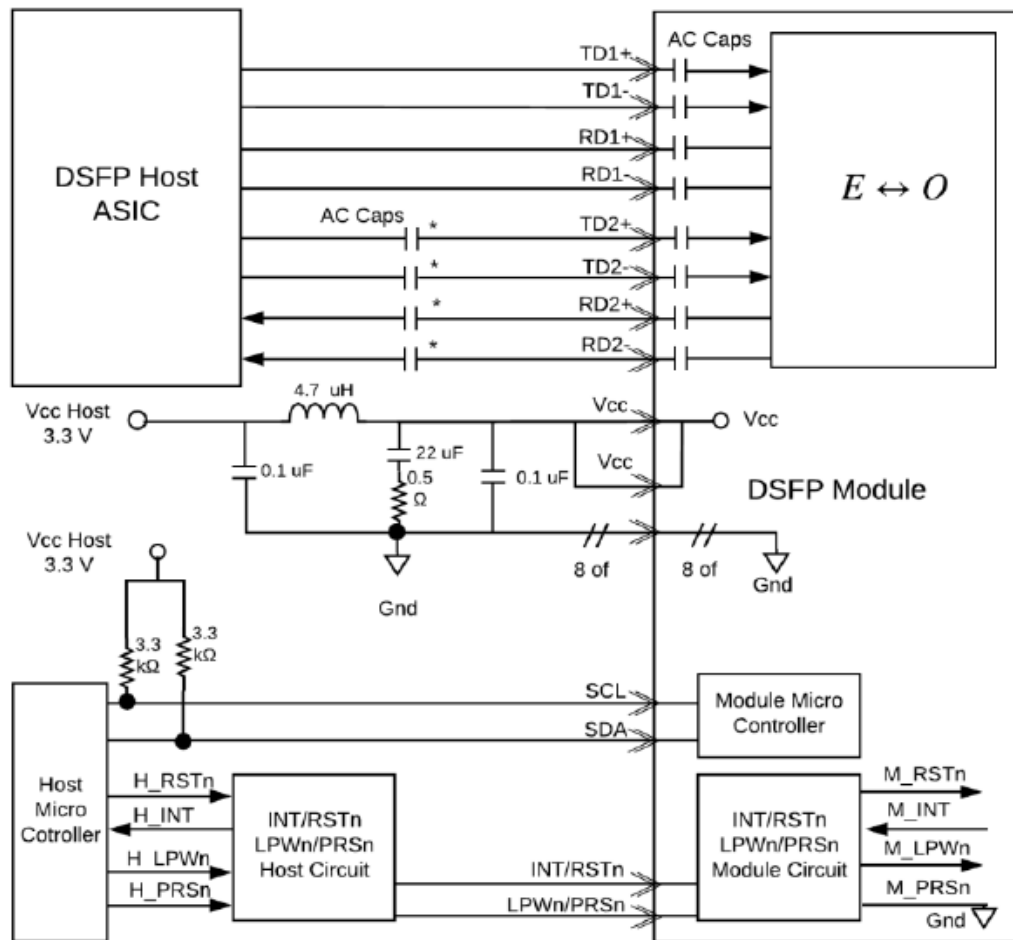
PIN Function Definitions

Pad	Logic	Symbol	Name/Description	Note
1	CML-I	TD2-	Transmitter Inverted Data Input Lane 2	
2	CML-I	TD2+	Transmitter Non-Inverted Data Input Lane 2	
3		Gnd	Module Ground	4
4	LVTTL-I/O	SDA	2-wire Serial Interface Data Line	
5	LVTTL-I/O	SCL	2-wire Serial Interface Clock	
6	Multi-level-I/O	LPWn/PRSn	Low Power Mode/Module Present (Mod_Abs)	
7		Gnd	Module Ground	4
8	CML-O	RD2+	Receiver Non-Inverted Data Output Lane 2	
9	CML-O	RD2-	Receiver Inverted Data Output Lane 2	
10		Gnd	Module Ground	4
11		Gnd	Module Ground	4
12	CML-O	RD1-	Receiver Inverted Data Output Lane 1	3
13	CML-O	RD1+	Receiver Non-Inverted Data Output Lane 1	3
14		Gnd	Module Ground	4
15		Vcc	Module 3.3 V Supply	
16		Vcc	Module 3.3 V Supply	
17		Gnd	Module Ground	4
18	CML-I	TD1+	Transmitter Non-Inverted Data Input Lane 1	3
19	CML-I	TD1-	Transmitter Inverted Data Input Lane 1	3
20		Gnd	Module Ground	4
21	Multi-level-I/O	INT/RSTn	Dual Function Module Interrupt and Reset Pin	
22		Gnd	Module Ground	4

Notes:

1. Labeling as inputs (I) and outputs (O) are from the perspective of the module.
2. The case makes electrical contact to the cage before any of the board edge contacts are made.
3. Backward compatible with SFF-8431 SFI interface.
4. The module ground contacts Gnd recommended to be isolated from the module case by offering flexibility in the host EMI control strategy.

Typical Interface Circuit



* Host AC Caps allow SFP+ backwards compatibility. If SFP+ modules will never be plugged in, the host AC Caps can be omitted.

Figure 1: Recommended Host Board Power Supply Filtering

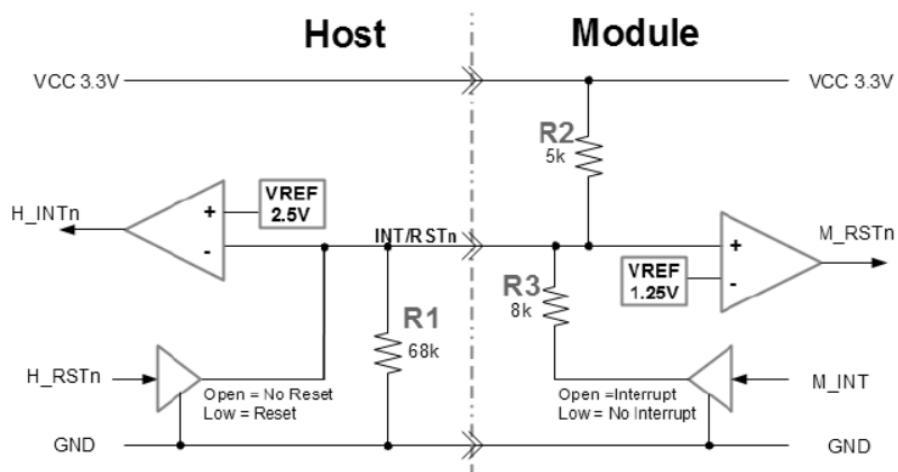


Figure 2: INT/RSTn circuit

Parameter	Nominal	Min.	Max.	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_INTn	2.500	2.475	2.525	Volts	Precision voltage reference for H_INTn
M_Vref_RSTn	1.250	1.238	1.263	Volts	Precision voltage reference for M_RSTn
R1	68k	66k	70k	Ohms	Recommend 68.1k ohms 1% resistor
R2	5k	4.9k	5.1k	Ohms	Recommend 4.99k ohms 1% resistor
R3	8k	7.8k	8.2k	Ohms	Recommend 8.06k ohms 1% resistor
V_INT/RSTn_1	0.000	0.000	1.000	Volts	INT/RSTn voltage for No Module
V_INT/RSTn_2	0.000	0.000	1.000	Volts	INT/RSTn voltage for Module installed, H_RSTn=Low
V_INT/RSTn_3	1.900	1.500	2.250	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=Low
V_INT/RSTn_4	3.000	2.750	3.465	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=High

Table 1: INT/RSTn circuit parameters

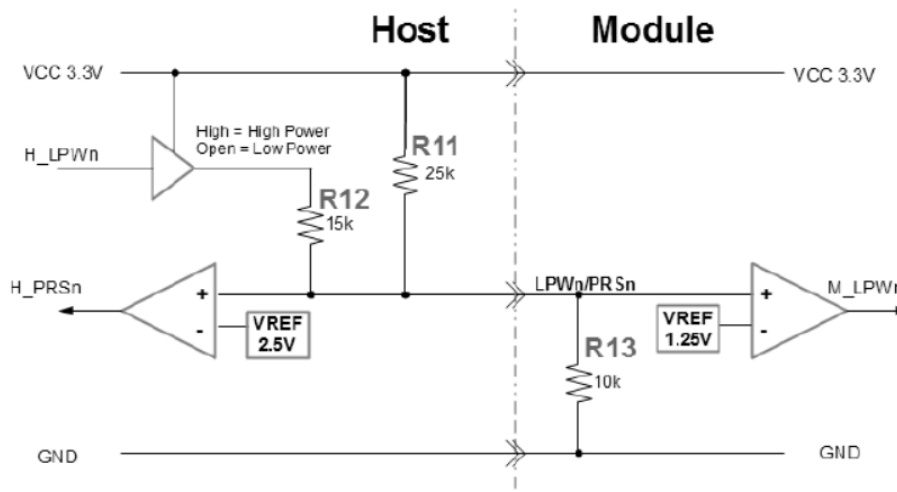


Figure 3: LPWn/PRSn circuit

Parameter	Nominal	Min.	Max.	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_PRSn	2.500	2.475	2.525	Volts	Precision voltage reference for H_PRSn
M_Vref_LPWn	1.250	1.238	1.263	Volts	Precision voltage reference for M_LPWn
R11	25k	24.5k	25.5k	Ohms	Recommend 24.9k ohms 1% resistor
R12	15k	14.7k	15.3k	Ohms	Recommend 15k ohms 1% resistor
R13	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
V_LPWn/PRSn_1	0.950	0.000	1.100	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=Low
V_LPWn/PRSn_2	1.700	1.400	2.250	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=High
V_LPWn/PRSn_3	3.300	2.750	3.465	Volts	LPWn/PRSn voltage for No Module
T_hplp			200	μs	High power mode to Low power mode transition time from assertion of LPWn or RSTn.

Table 2: LPWn/PRSn circuit parameters

Electrical Pad Layout

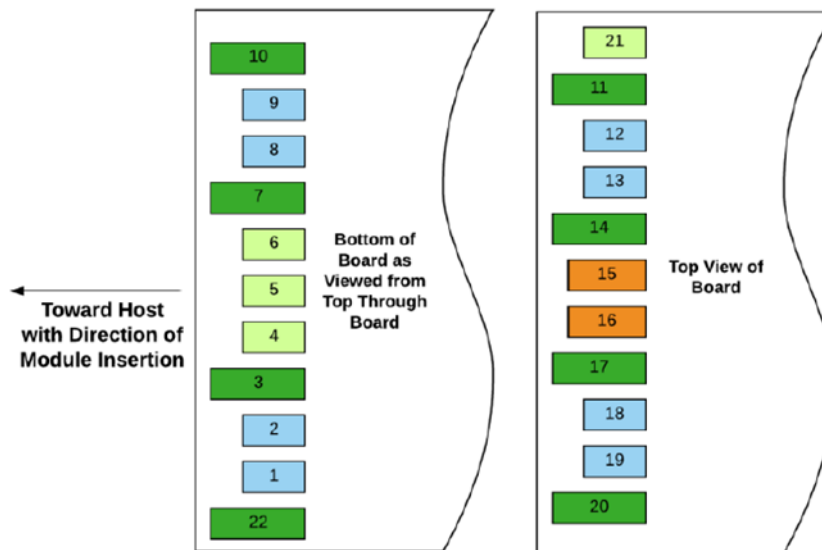
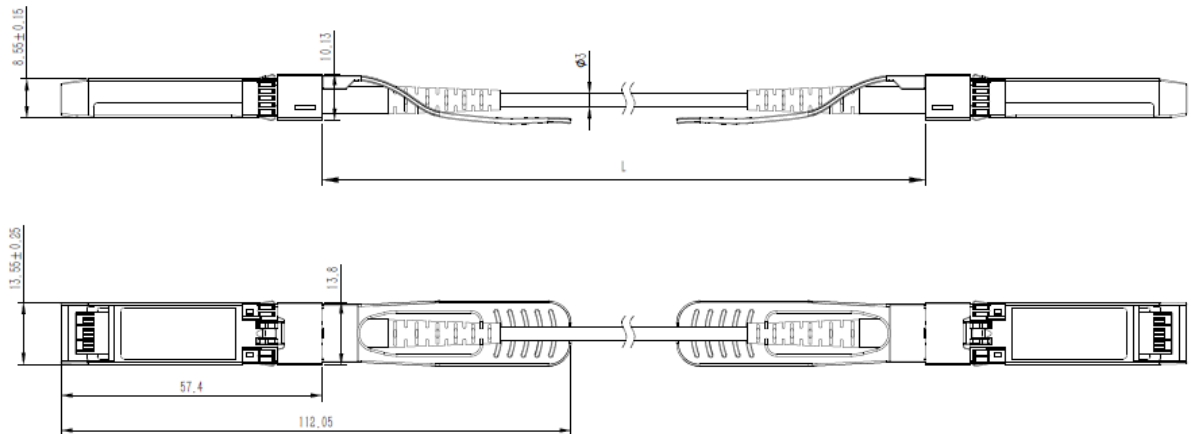


Figure 4: Module contact definition

Mechanical Specifications



ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Ordering Information

Ordering P/Ns	Description
DH88hh-GCCA-xxx	up to 100m, 850nm, MMF, DSFP AOC, Commercial temperature

XXX	Cable (MMF) Length
001	001=1m
⋮	⋮
050	050=50m
⋮	⋮
100	100=100m

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